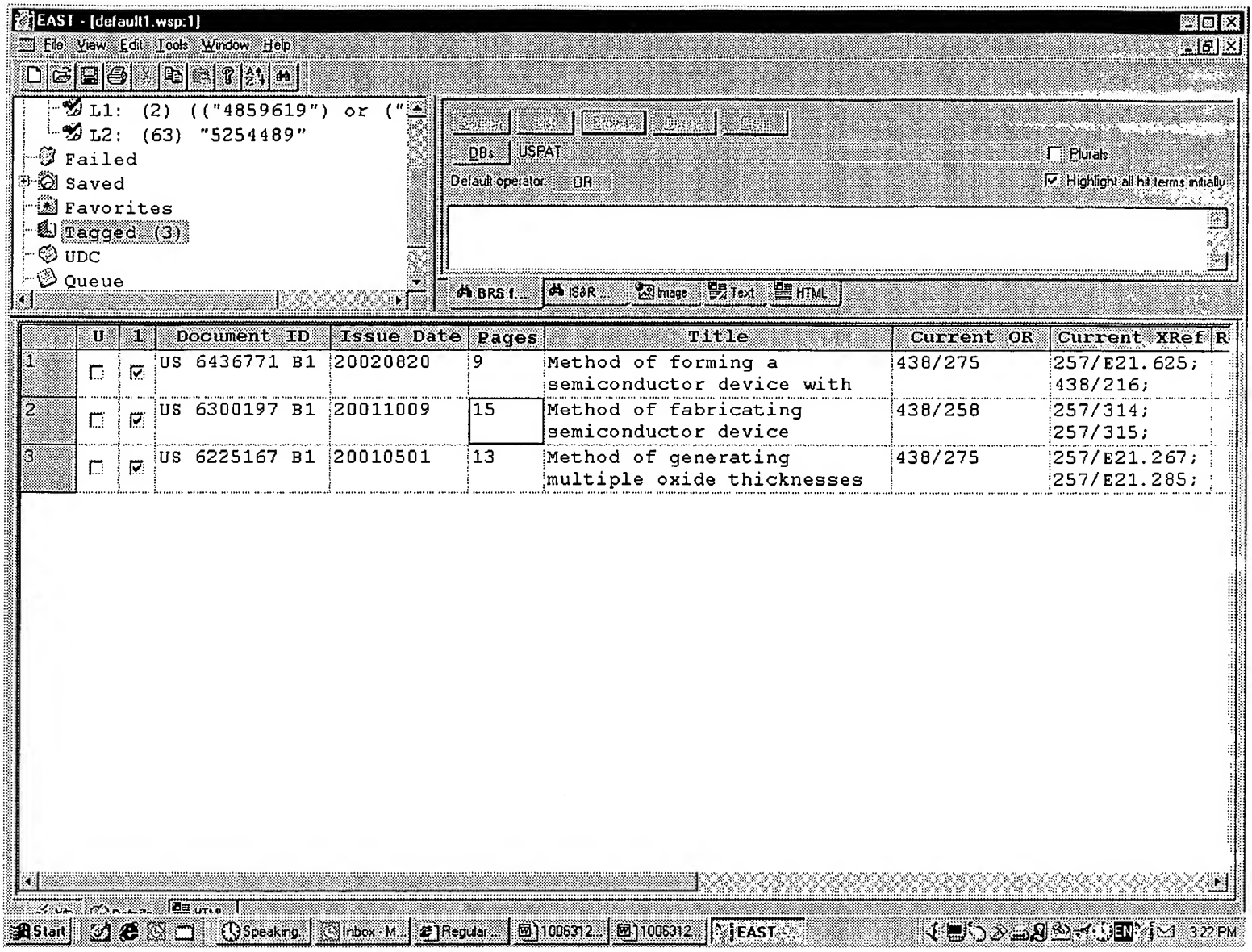


Notice of Allowability	Application No.	Applicant(s)	
	09/316,029	HONG ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication app ars on the cov r sh et with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed March 26, 2003.*.
2. ☒ The allowed claim(s) is/are *1,3-8,10,11 and 14-16*.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

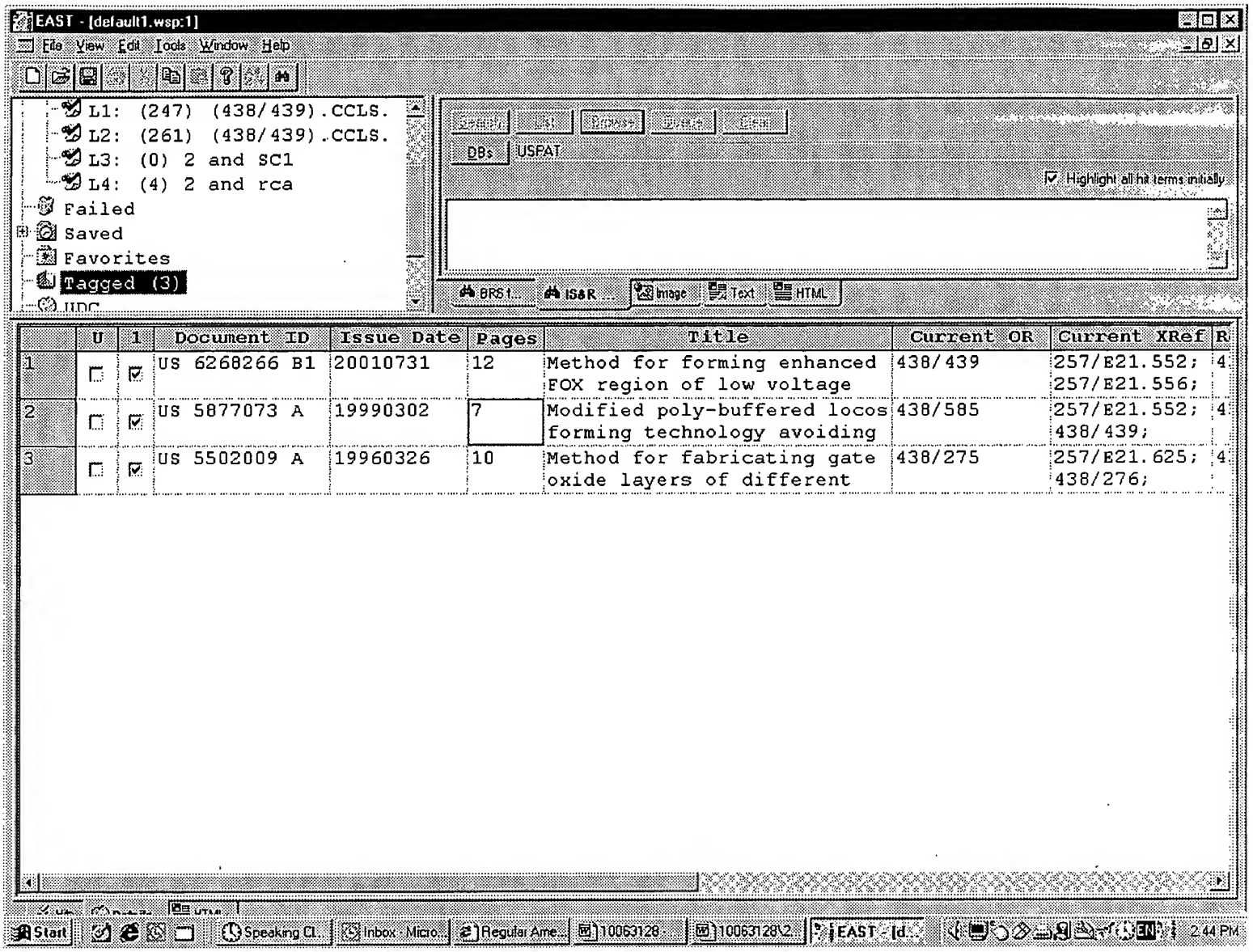
8. ☒ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☒ including changes required by the proposed drawing correction filed *17 July 2002*, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☐ Notice of References Cited (PTO-892)
2☐ Notice of Informal Patent Application (PTO-152)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
4☐ Interview Summary (PTO-413), Paper No.____ .
5☐ Information Disclosure Statements (PTO-1449), Paper No. ____.
6☐ Examiner's Amendment/Comment
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other .



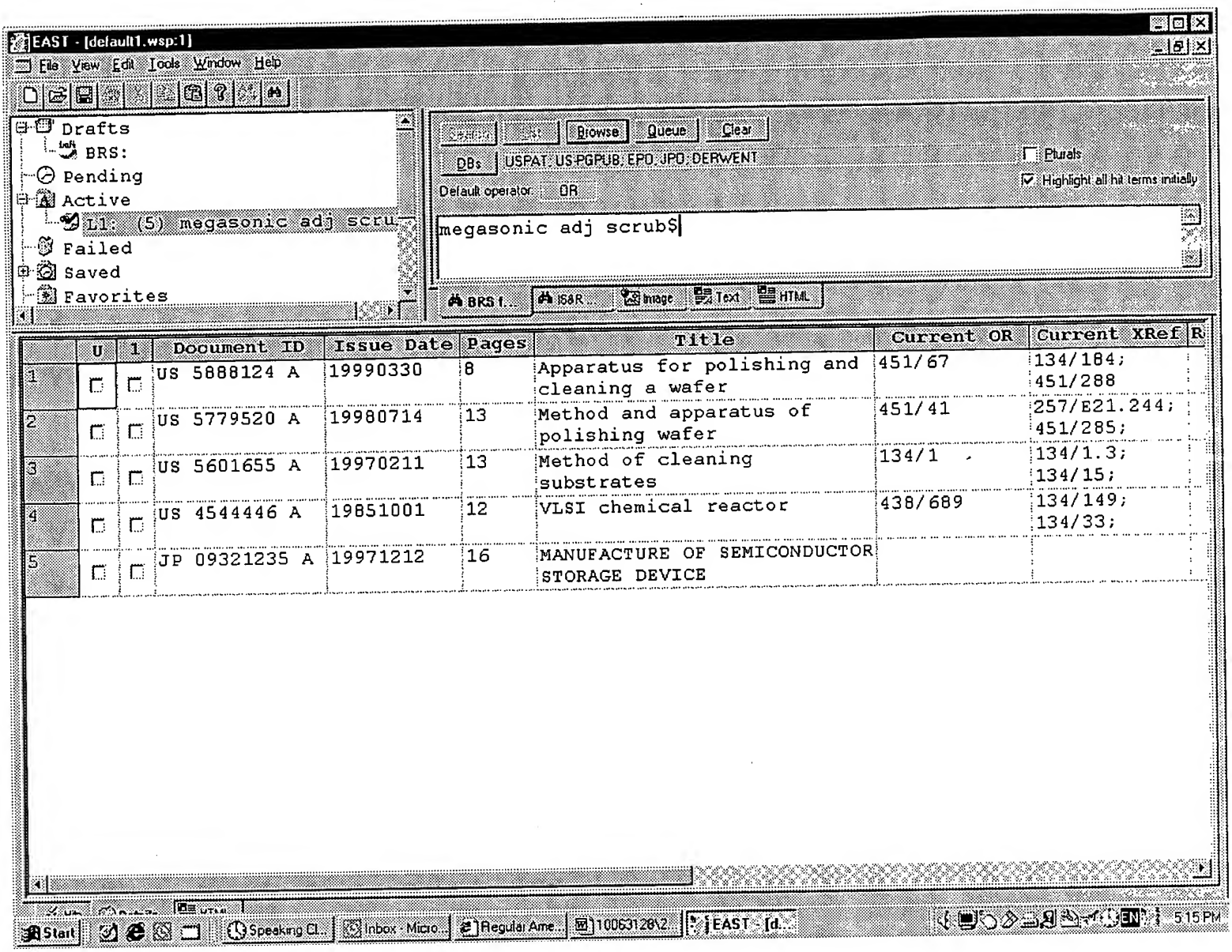
	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☑	US 6268266 B1	20010731	12	Method for forming enhanced FOX region of low voltage	438/439	257/E21.552; 257/E21.556;	4
2	☐	☑	US 5877073 A	19990302	7	Modified poly-buffered locos forming technology avoiding	438/585	257/E21.552; 438/439;	4
3	☐	☑	US 5502009 A	19960326	10	Method for fabricating gate oxide layers of different	438/275	257/E21.625; 438/276;	4

09/803434
09/996570

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
April 16, 2003



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 5888124 A	19990330	8	Apparatus for polishing and cleaning a wafer	451/67	134/184; 451/288	
2	☐	☐	US 5779520 A	19980714	13	Method and apparatus of polishing wafer	451/41	257/E21.244; 451/285;	
3	☐	☐	US 5601655 A	19970211	13	Method of cleaning substrates	134/1	134/1.3; 134/15;	
4	☐	☐	US 4544446 A	19851001	12	VLSI chemical reactor	438/689	134/149; 134/33;	
5	☐	☐	JP 09321235 A	19971212	16	MANUFACTURE OF SEMICONDUCTOR STORAGE DEVICE			

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Summary

Document	Pages	Printed	Missed	Copies
US006436771	9	9	0	1
US006225167	13	13	0	1
Total (2)	22	22	0	-

US006207509B1

(12) **United States Patent**
Inoue

(10) **Patent No.: US 6,207,509 B1**
(45) **Date of Patent: Mar. 27, 2001**

(54) **METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE**

(75) Inventor: **Tatsuro Inoue**, Tokyo (JP)

(73) Assignee: **NEC Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/357,298**

(22) Filed: **Jul. 20, 1999**

(30) **Foreign Application Priority Data**

Jul. 21, 1998 (JP) 10-204841

(51) **Int. Cl.**[7] **H01L 21/8234**
(52) **U.S. Cl.** **438/275**; 428/257; 428/263
(58) **Field of Search** 438/275, 263, 438/264, 257, 258, 261, 298, 541, 542

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,254,489 * 10/1993 Nakata 438/241
5,466,622 * 11/1995 Cappelleti 438/287
5,553,017 * 9/1996 Ghezzi et al. 257/314
5,668,035 * 9/1997 Fang et al. 438/239

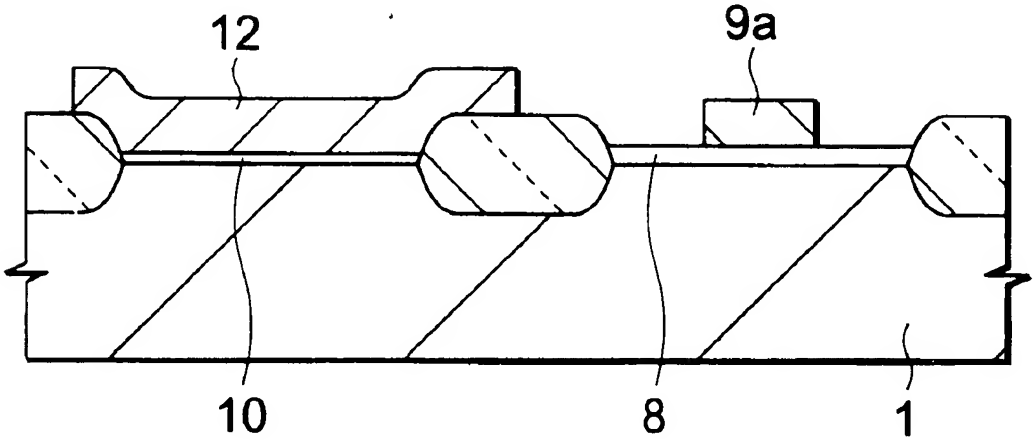
* cited by examiner

Primary Examiner—David Nelms
Assistant Examiner—Dung Anh Le
(74) *Attorney, Agent, or Firm*—Young & Thompson

(57) **ABSTRACT**

In a method of manufacturing a semiconductor device, a first sacrifice oxide film is formed on a substrate. Next, a second sacrifice oxide film is formed on the substrate by etching the first sacrifice oxide film to a predetermined depth in a first etching process. Herein, the second sacrifice oxide film is thinner than the first sacrifice oxide film. Subsequently, the second sacrifice oxide film is completely removed from a surface of the substrate in a second etching process so as to expose the surface of the substrate. Finally, an oxide film is formed on the exposed surface of the substrate.

15 Claims, 7 Drawing Sheets



If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
April 16, 2003

(14)

US005254489A

United States Patent [19]

Nakata

[11] Patent Number: 5,254,489

[45] Date of Patent: Oct. 19, 1993

[54] METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE BY FORMING FIRST AND SECOND OXIDE FILMS BY USE OF NITRIDATION

[75] Inventor: Hidetoshi Nakata, Tokyo, Japan

[73] Assignee: NEC Corporation, Tokyo, Japan

[21] Appl. No.: 779,078

[22] Filed: Oct. 18, 1991

[30] Foreign Application Priority Data

Oct. 18, 1990 [JP] Japan 2-280393
Nov. 30, 1990 [JP] Japan 2-340916

[51] Int. Cl.[5] H01L 21/265

[52] U.S. Cl. 437/40; 437/43; 148/DIG. 112; 148/DIG. 117

[58] Field of Search ..... 437/40, 41, 43, 241, 437/247, 979, 983; 148/DIG. 112, DIG. 114, DIG. 116, DIG. 117

[56] References Cited

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4,113,515 9/1978 Kooi et al. 148/DIG. 114
4,621,277 11/1986 Ito et al. 148/DIG. 112
4,651,406 3/1987 Shimizu et al. 437/43
4,971,923 11/1990 Nakanishi 437/69

FOREIGN PATENT DOCUMENTS

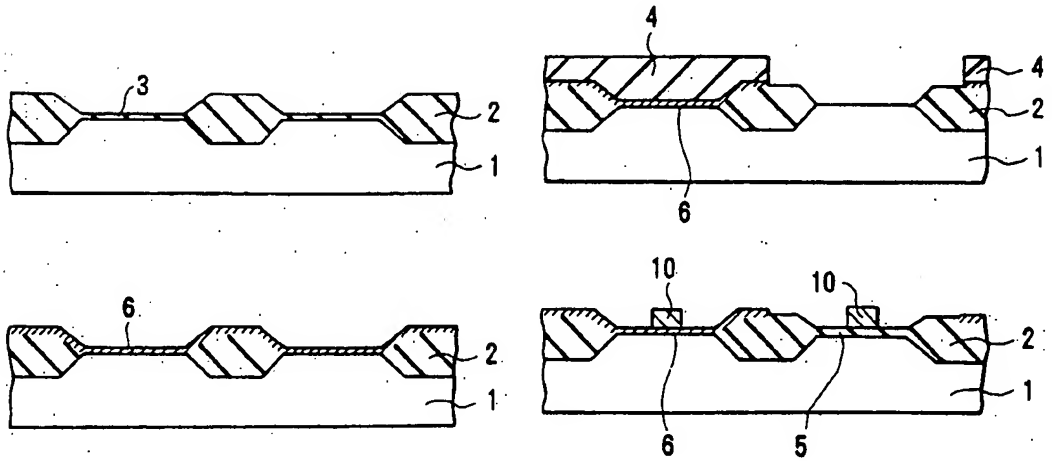
62-256476 11/1987 Japan .
8603621 6/1986 World Int. Prop. O. 148/DIG. 114

Primary Examiner—Brian E. Hearn
Assistant Examiner—C. Chaudhari
Attorney, Agent, or Firm—Sughrue, Mion, Zinn, Macpeak & Seas

[57] ABSTRACT

According to this invention, there is provided a method of manufacturing a semiconductor device. An element region and an element isolation region are formed on a semiconductor substrate of a first conductivity type. A first oxide film prospectively serving as a gate insulating film is formed in the element region. Thermal oxidization is performed after annealing is performed in nitrogen or ammonia atmosphere to nitrify an entire surface of the first oxide film. A predetermined region of a nitrified first oxide film is removed, and a second oxide film prospectively serving as a gate insulating film is formed in the predetermined region using the nitrified first oxide film as a mask. A gate electrode constituted by a polysilicon film is formed on each of the nitrified first oxide film and the second oxide film.

13 Claims, 9 Drawing Sheets



DETAILED ACTION

Amendment

1. Amendment filed March 26, 2003 has been entered as Paper No. 27. Claims 2, 12 and 13 have been cancelled. Claims 1 and 3 have been amended. Claims 1, 3-8, 10, 11 and 14-16 are pending.

Allowable Subject Matter

2. Claims 1, 3-8, 10, 11 and 14-16 are allowed.

3. The following is an examiner's statement of reasons for allowance: prior art of record fails to teach a method for forming a trench type isolation film in a semiconductor device including: performing the first anneal after filling the trench; performing the second anneal after planarizing the trench fill and removing the mask layer after the second anneal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.